

REMARKS

Summary of Claim Status

Claims 1-19 are pending in the present application, and are rejected for the reasons discussed below. Applicants gratefully acknowledge the telephone conference with the representative for Applicants, John King, and the Examiner on November 3, 2006. Applicants respectfully request favorable reconsideration of the claims and withdrawal of the pending rejections in view of the present amendments and in light of the following discussion.

Rejections Under 35 U.S.C. § 102

Claims 1-5 and 7-11 are rejected under 35 U.S.C. § 102(b) as being anticipated by Jain, U.S. Patent No. 6,038,386 ("Jain"). In response to the rejection, Applicants have amended Claim 1 to overcome the rejection. In particular, Applicants have amended Claim 1 to indicate that the programmable logic device has a plurality of active blocks, where each active block has a plurality of paths. Applicants have further amended the step of determining a plurality of timing slacks to indicate that the plurality of timing slacks is associated with a plurality of paths of an active block for each of the active blocks. Finally, Applicants have added a step of enabling, for each active block, the assignment of either of a first supply voltage or a second supply voltage to operate the active block. Applicants respectfully submit that Claim 1 as amended clearly distinguishes over Jain.

Jain teaches determining the maximum number of Macrocells that can be switched to low power, depending upon the additional delay incurred for switching a Macrocell to low power. See Jain at Col. 12, line 63 to Col. 13, line 42. However, Jain teaches that an individual Macrocell may be switched to low power, depending upon the impact of switching the power on the various paths that share the Macrocell. That is, a decision to switch a Macrocell to low power depends upon timing constraints of a number of paths. As shown in the example of Fig. 12 of Jain, described starting at Col. 15, line 55, the determination to provide a reduced voltage to an individual

Macrocell is based upon the slack times of all of the paths, and the respective number of product terms (P-terms) for the Macrocells. For example, a Macrocell in a path having the greatest number of P-terms may be switched to low power assuming that the switching does not violate a constraint requirement of any path sharing the Macrocell. In contrast, the method of Claim 1 indicates that each active block has a plurality of paths, and that a plurality of timing slacks are associated with the plurality of paths of an active block. Further, Applicants claim enabling, for each active block, the assignment of either of a first supply voltage or a second supply voltage to operate the active block based upon the minimum timing slack for each active block. Therefore, in contrast to the selection of low power for an individual Macrocell in a given path, Applicants claim selecting one of a first and second supply voltage for an active block based upon a minimum timing slack for a plurality of paths of the active block. Applicants believe Claim 1 as amended is allowable over Jain, and respectfully request reconsideration of the rejection of Claim 1.

Claims 2-5 and 7-11 depend, either directly or indirectly, from Claim 1, and thus include all of the limitations of Claim 1. Therefore, for at least the same reasons, Applicants believe that Claims 2-5 and 7-11 are also allowable, and respectfully request reconsideration of the rejection of Claims 2-5 and 7-11.

All of the above amendments are fully supported by the specification, at least for example in Figs. 7 and 8 and the corresponding text.

Rejections Under 35 U.S.C. § 103

Claims 6 and 12-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jain in view of Mizuno et al., U.S. Patent Publication No. 2004/0145955 ("Mizuno"). With respect to Claim 6, which depends from Claim 1, Applicants believe the present amendment to Claim 1 overcomes the rejection. That is, while Mizuno is cited for disclosing the use of a third voltage source, Mizuno also fails to disclose or suggest the steps of Claim 1 which are not disclosed by Jain. Accordingly, Claim 6 is further believed to be allowable, and Applicants respectfully request reconsideration of the rejection of Claim 6.

With respect to Claim 12, Applicants have amended Claim 12 to indicate that the plurality of timing slacks is associated with a plurality of paths of a programmable logic block, and that each of the programmable logic blocks receives a selected one of a plurality of operating voltages. Applicants have further amended Claim 12 to indicate that each variable voltage regulator selects one of the plurality of operating voltages for the corresponding one of the programmable logic blocks. Finally, Applicants have amended Claim 12 to indicate that the means for controlling the variable voltage regulators provides an operating voltage to the corresponding one of the programmable logic blocks in response to the minimum timing slack associated with the corresponding one of the programmable logic blocks. Support for the amendments may be found at least in Figs. 7 and 9 and the corresponding text.

As noted above, Jain does not disclose or suggest determining a minimum timing slack associated with a plurality of paths of a programmable logic block, or selecting one of a plurality of operating voltages for a programmable logic block, wherein the operating voltage is selected in response to the minimum timing slack associated with the programmable logic block. While Mizuno is cited for disclosing a plurality of variable voltage regulators, Mizuno also fails to disclose or suggest determining a minimum timing slack associated with a plurality of paths of a programmable logic block, or selecting one of a plurality of operating voltages for a programmable logic block in response to the minimum timing slack. Applicants respectfully submit that Claim 12 as amended clearly distinguishes over the combination of Jain and Mizuno, and respectfully request reconsideration of the rejection of Claim 12.

Claims 13 and 14 depend from Claim 12, and thus include all of the limitations of Claim 12. Therefore, for at least the same reasons, Applicants believe Claims 13 and 14 are also allowable, and respectfully request reconsideration of the rejection of Claims 13 and 14.

Claims 15-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jain in view of Mizuno and further in view of Almulla, U.S. Patent No. 5,612,892. Claim 15 depends from Claim 12, and thus includes all of the limitations of Claim 12.

Almulla is cited for disclosing the use of switches between both a high power signal path and a low power signal path and a circuit. However, Almulla also fails to disclose or suggest determining a minimum timing slack associated with a plurality of paths of a programmable logic block, or selecting one of a plurality of operating voltages for a programmable logic block in response to the minimum timing slack associated with the programmable logic block. Therefore, for at least the same reasons, Applicants believe that Claim 15 is also allowable, and respectfully request reconsideration of the rejection of Claim 15.

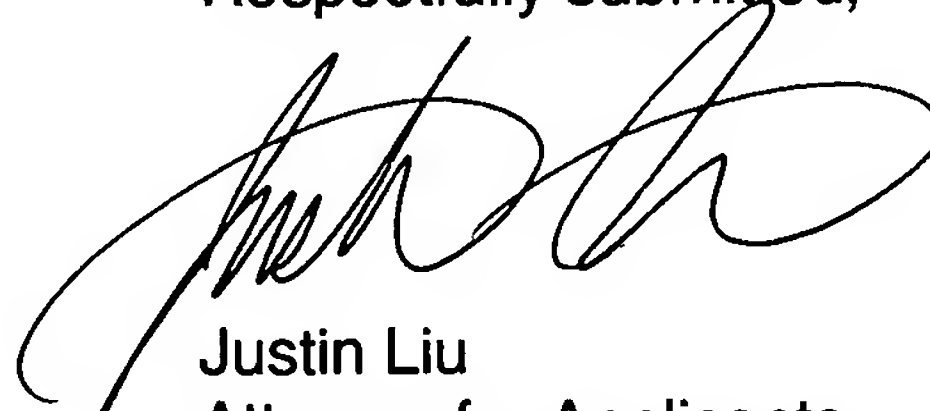
Finally, Applicants have amended Claim 16 to indicate that the corresponding plurality of timing slacks is associated with a plurality of paths of a programmable logic block. Applicants have further amended the means for controlling the first and second voltage switches to indicate that each programmable logic block is coupled to receive one of the first voltage supply and the second voltage supply. Support for the amendments may be found at least in Figs. 7 and 8 and the corresponding text. As set forth above, Jain fails to disclose or suggest a programmable logic block which is coupled to receive one of a first supply voltage or a second supply voltage based upon an associated minimum timing slack. While there is no statement in the Office Action as to how Mizuno is applied in Claim 16, Almulla is cited for disclosing the plurality of first voltage switches and the plurality of second voltage switches, and the means for controlling the voltage switches. However, Almulla also fail to disclose or suggest the selection of a first and second voltage supply as claimed. That is, Almulla fails to disclose or suggest a programmable logic block which is coupled to receive one of a first supply voltage or a second supply voltage based upon an minimum timing slack associated with a plurality of paths of the programmable logic block. Applicants respectfully submit that Claim 16 as amended clearly distinguishes over the references, and respectfully request reconsideration of Claim 16.

Claims 17-19 depend from Claim 16, and thus include all of the limitations of Claim 16. Therefore, for at least the same reasons, Applicants believe Claims 17-19 are also allowable, and respectfully request reconsideration of the rejection of Claims 17-19.

Conclusion

No new matter has been introduced by any of the above amendments. In light of the above amendments and remarks, Applicants believe that Claims 1-19 are in condition for allowance, and allowance of the application is therefore requested. If action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicants' attorney, Justin Liu, at 408-879-4641.

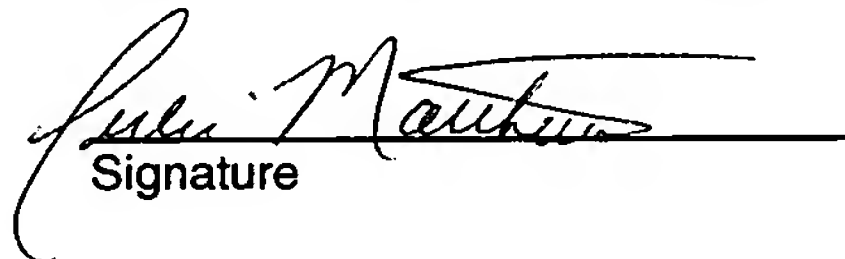
Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, November 10, 2006.

Julie Matthews
Name


Signature